REMARKS

The above-referenced patent application (hereinafter "application") has been reviewed in light of the Office Action, dated December 30, 1999, in which: claims 13-20 are withdrawn from consideration; claims 1-12 and 21-26 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Tran et al. (U.S. Patent 5,780,883); and claims 1-12 and 21-26 are also rejected under 35 U.S.C § 103(a) as being unpatentable over Sato (U.S. Patent 4,816,887). Consideration of the above-referenced patent application in view of the following remarks is respectfully requested.

Claims 1-12 and 21-26 are pending the application. No claims have been cancelled or amended. No new claims have been added.

Multiple informalities and two minor omissions are noted in the specification. These minor errors and omissions were made inadvertently and without deceptive intent. Appropriate corrections have been made by the foregoing amendments. It is respectfully requested that the Examiner approve and enter these minor corrections.

The Examiner has withdrawn claims 13-20 from consideration in accordance with Applicant's response, mailed on November 15, 1999. In this response, Applicant elected claim group I as set forth by the Examiner in the previous Office Action, mailed on October 14, 1999. The Examiner has treated this election as an election without traversal under MPEP § 818.03(a). This action by the Examiner is respectfully noted, however, Applicant reserves the right to pursue these claims in a divisional application under 35 U.S.C. § 121.

The Examiner has rejected claims 1-12 and 21-26 under 35 U.S.C. § 103(a) as being unpatentable over Tran et al. (hereafter "Tran"). This rejection by the Examiner is respectfully traversed.

Claim 1 of the application specifically states:

> An integrated circuit comprising: a gate array architecture;
> said gate array architecture including a semiconductor substrate having a plurality of N-type diffusion regions and P-type diffusion regions; said diffusion regions having partially overlying polysilicon landing sites to form N-type and P-type transistors;
> wherein the regions are relatively-sized to form two distinct transistor sizes, smaller N- and P-type transistors and larger N- and P-type transistors.

In his rejection of claim 1, the Examiner states that "Tran discloses...a gate array architecture comprising a plurality of N-type and P-type diffusion regions having polysilicon gates in which the regions have two distinct transistor sizes, smaller N and P type transistors and larger N and P type transistors." Applicant respectfully asserts that the Examiner's rejection on this basis is improper.

Applicant respectfully asserts that claim 1 patentably distinguishes from Tran in a number of respects. For example, claim 1, quoted above, recites "**diffusion regions having partially overlying polysilicon landing sites to form N-typ and P-type transistors**." Examination of Tran, particularly FIGs. 3A and 3B, demonstrates that the cited patent does not suggest or disclose the invention as recited in claim 1. Instead, Tran shows diffusion regions having isolated **non-overlying** polysilicon landing sites.

The configuration disclosed by Tran is disadvantageous in a number of respects. For example, the power consumption savings and design implementation benefits that may be achieved by embodiments in accordance with the invention, such as described in the specification on page 5, lines 21-28, and illustrated by FIG. 5 may not be achieved by Tran. **For example, at a minimum, the structures disclosed in the cited patent may require additional design layout complexity to achieve any power consumption benefit. This additional design complexity my result in requiring, at a minimum, an additional layer of metal routing. This additional metal routing may, in turn, offset, at least a portion of, any reduction in power consumption due to the increased parasitic impedance of such metal routing.**

Based on the foregoing, it is respectfully asserted that Tran would not render claim 1 obvious to one of ordinary skill in the art. Specifically, one of ordinary skill having this patent before him or her would be unable to produce the invention as recited in claim 1. Therefore, it is respectfully requested that the Examiner withdraw his rejection of claim 1.

Claims 2-12 depend from and include all the limitations of claim 1. Therefore, it is respectfully asserted that these claims distinguish from the cited patent on the same basis as claim 1. It is respectfully requested that the Examiner withdraw his rejection of claims 2-12.

The Examiner has also rejected claim 21 under 35 U.S.C. § 103(a) on Tran. Without addressing the merits of the Examiner's comments regarding claim 21, which are, therefore, not conceded, Applicant respectfully points out that claim 21 contains similar limitations to those discussed above with respect to claim 1. Therefore, it is respectfully asserted that claim 21 patently distinguishes from Tran for similar reasons as discussed above regarding claim 1. It is respectfully requested that the Examiner withdraw his rejection of claim 21.

Claims 22-26 depend from and include all the limitations of claim 21. Therefore, it is respectfully asserted that these claims distinguish from the cited patent on the same basis as claim 21. It is respectfully requested that the Examiner withdraw his rejection of claims 22-26.

The Examiner has rejected claims 1-12 and 21-26 under 35 U.S.C. § 103(a) as being unpatentable over Sato. This rejection by the Examiner is respectfully traversed.

It is respectfully asserted that the Examiner's rejection with respect to these claims is procedurally insufficient. In this regard, MPEP § 706 specifically states that "[t]he goal of examination is to clearly articulate any rejection early in the prosecution process so that the applicant has the opportunity to provide evidence of patentability and otherwise respond completely at the earliest opportunity." However, the Examiner merely states in the Detailed Action that "Sato discloses a gate array having two distinct transistor sizes on the order of one-third. It would have been obvious that Sato discloses the claimed device."

It is respectfully asserted that the Examiner has failed to adequately articulate the basis for his rejection under 35 U.S.C. § 103(a) as required by the MPEP. Because the Examiner has failed to clearly articulate the basis for his rejection, other than a broad reference to the cited patent, Applicant has been placed in the unfair position of speculating or guessing as to the basis for the Examiner's rejection. In this regard, it is impossible for Applicant to be certain of the "reasons" that the Examiner may have for believing the cited patent renders claim 1, for example, obvious. Therefore, the examination goals that are articulated in MPEP § 706 have been frustrated.

Notwithstanding the procedural insufficiency of the Examiner's rejection, Applicant now proceeds to the merits with respect to the Examiner's rejection because it is respectfully asserted that that claim 1 patentably distinguishes from Sato. In this respect, Applicant respectfully asserts that claim 1 distinguishes from Sato for, at least, reasons similar to those discussed above with respect to Tran, such as non-overlying polysilicon landing sites, design advantages and potential power consumption benefits. Therefore, it is respectfully requested that the Examiner withdraw his rejection of claim 1.

Claims 2-12 depend from and include all the limitations of claim 1. Therefore, it is respectfully asserted that these claims distinguish from the cited patent on the same basis as claim 1. It is respectfully requested that the Examiner withdraw his rejection of claims 2-12.

The Examiner has also rejected claim 21 under 35 U.S.C. § 103(a) on Sato on the same basis as claim 1. Therefore, the arguments made regarding the procedural insufficiency of the Examiner's rejection with respect to claim 1 are relevant and apply here as well. Applicant also respectfully points out that claim 21 contains similar limitations to those discussed above with respect to claim 1. Therefore, it is respectfully asserted that claim 21 patentably distinguishes from Sato for similar reasons as discussed above regarding claim 1. It is respectfully requested that the Examiner withdraw his rejection of claim 21.

Claims 22-26 depend from and include all the limitations of claim 21. Therefore, it is respectfully asserted that these claims distinguish from the cited patent on the same basis as claim 21. It is respectfully requested that the Examiner withdraw his rejection of claims 22-26.

CONCLUSION

In view of the foregoing, it is respectfully asserted that all of the claims pending in this patent application, as amended, are in condition for allowance. If the Examiner has any questions, he is invited to contact the undersigned at (503) 264-0967. Reconsideration of this patent application and early allowance of all the claims, as amended, is respectfully requested.

Respectfully submitted,

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